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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,775	08/08/2006	Yasuhiro Okamoto	Q96219	9772
23373 7590 06/23/2008 SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER LL MEIYA	
			ART UNIT 2811	PAPER NUMBER
			MAIL DATE 06/23/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/588,775

**Applicant(s)**

OKAMOTO ET AL.

**Examiner**

MEIYA LI

**Art Unit**

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE \_\_\_\_\_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_\_.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) \_\_\_\_\_ is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Information Disclosure Statement***

1. The information disclosure statement (IDS) submitted on June 2, 2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9, 10, 12-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. The claimed limitations of "the size of said field plate portion do not exceed 70% of an interval between said gate electrode and said drain electrode", as recited in claims 9 and 10, is unclear because the field plate portion has three dimensions.

5. The claimed limitations of "the entire size of said field plate portion ...", as recited in claims 12-15, is unclear because the field plate portion has three dimensions.

***Claim Rejections - 35 USC § 103***

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
7. Claims 1-2, 4, 6-10, and 12-15, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshimoto (JP56088364) in view of Shur et al. (2005/0087752).

As for claims 1 and 4, Toshimoto shows in Fig. 2 and related texts (see, i.e. Abstract) a field effect transistor comprising:

- a semiconductor layer structure 8;
- a source electrode 14 and a drain electrode 13 (right portion) that are so formed on said semiconductor layer structure 8 as to be separated from each other,
- a gate electrode 12 formed between said source electrode 14 and said drain electrode 13 (right portion); and
- an insulating film 11 formed on said semiconductor layer structure 10,

wherein said gate electrode 12 has a field plate portion that projects towards said drain electrode 9 in the form of an eave and that is formed on said insulating film 11;

wherein a thickness C of a portion of said insulating film 11 lying between said field plate portion and said semiconductor layer structure 10 gradually increases from said gate electrode 12 toward said drain electrode 13 (right portion), and

wherein said thickness C of said portion of said insulating film 11 varies continuously.

Toshimoto does not state that semiconductor structure is a III group nitride semiconductor layer structure including hetero junction.

Shur et al. teach a III group nitride semiconductor layer structure including hetero junction ([0025], lines 6-8 and 15-17; [0033], lines 5-6).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the hetero junction III group nitride semiconductor layer structure, as taught by Shur et al., in Toshimoto's device, in order to reduce the resistance, provide a higher output power and a better noise characteristic.

As for claim 2, the prior art combined device shows structure has an AlGaIn/GaN hetero structure (Shur: [0025], lines 6-8 and 15-17).

As for claim 6, the prior art combined device shows said insulating film is a SiO<sub>2</sub> film or a SiN film (Shur: [0029], lines 8-9).

As for claim 7, the prior art combined device shows said insulating film is a laminated layer of a SiO<sub>2</sub> film and a SiN film (Shur: [0029], lines 8-9).

As for claim 8, the prior art combined device shows a drain field plate electrode 13 (left portion) connected to said drain electrode 13 (right portion) is arranged on said insulating film 11 between said gate electrode 12 and said drain electrode 13 (right portion) (Toshimoto: Fig. 2).

As for claims 9 and 10, Toshimoto and Shur et al. disclosed substantially the entire claimed invention, as applied to claims 1 and 4 above, except the size of said field plate portion does not exceed 70% of an interval between said gate electrode and said drain electrode.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include the size of said field plate portion does not exceed 70% of an interval between said gate electrode and said drain electrode, in order to optimize the performance of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Furthermore, it has been held in that the applicant must show that a particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Note that the law is replete with cases in which when the mere difference between the claimed invention and the prior art is some dimensional limitation or other variable within the claims, patentability cannot be found. The instant disclosure does not set forth evidence ascribing unexpected results due to the claimed dimensions. See *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338 (Fed. Cir. 1984), which held that the dimensional limitations failed to point out a feature which performed and operated any differently from the prior art.

As for claims 12-15, Toshimoto and Shur et al. disclosed substantially the entire claimed invention, as applied to claims 1 and 4 above, except the entire size of said field plate portion that extends to said drain electrode is 0.5  $\mu\text{m}$  or more and preferably 0.7  $\mu\text{m}$  or more.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include the entire size of said field plate portion that extends to said drain electrode is 0.5  $\mu\text{m}$  or more and preferably 0.7  $\mu\text{m}$  or more, in order to optimize the performance of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Furthermore, it has been held in that the applicant must show that a particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Note that the law is replete with cases in which when the mere difference between the claimed invention and the prior art is some dimensional limitation or other variable within the claims, patentability cannot be found. The instant disclosure does not set forth evidence ascribing unexpected results due to the claimed dimensions. See *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338 (Fed. Cir. 1984), which held that the dimensional limitations failed to point out a feature which performed and operated any differently from the prior art.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toshimoto (JP56088364) and Shur et al. (2005/0087752), as applied to claim 1 above, in view of Riccobene (6,229,184).

Toshimoto and Shur et al. disclosed substantially the entire claimed invention, as applied to claim 1 above, except a thickness of said field plate portion gradually decreases from said gate electrode toward said drain electrode.

Riccobene teaches a thickness of said field plate portion gradually decreases from said gate electrode toward said drain electrode (Fig. 1).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include a thickness of said field plate portion gradually decreases from said gate electrode toward said drain electrode, as taught by Riccobene, in Toshimoto and Shur et al.'s device, in order to reduce capacitance and increase circuit speed.

9. Claims 1-3, 6-9, 12, and 14, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirai (5,422,505) in view of Shur et al. (2005/0087752).

As for claim 1, Shirai shows in Fig. 1 and related text (see, i.e. Cols. 2-3) a field effect transistor comprising:

a semiconductor layer structure 10;

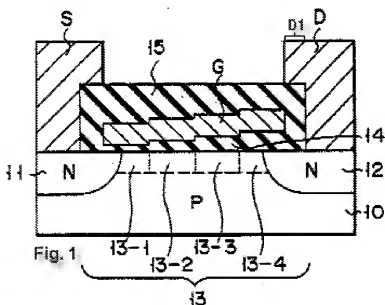
a source electrode S and a drain electrode D that are so formed on said semiconductor layer structure 10 as to be separated from each other,

a gate electrode G formed between said source electrode S and said drain electrode D; and

an insulating film 14 formed on said semiconductor layer structure 10,

wherein said gate electrode G has a field plate portion that projects towards said drain electrode D in the form of an eave and that is formed on said insulating film 14; and

wherein a thickness of a portion of said insulating film 14 lying between said field plate portion and said semiconductor layer structure 10 gradually increases from said gate electrode G toward said drain electrode D.



Shirai does not state that semiconductor structure is a III group nitride semiconductor layer structure including hetero junction.

Shur et al. teach a III group nitride semiconductor layer structure including hetero junction ([0025], lines 6-8 and 15-17; [0033], lines 5-6).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the hetero junction III group nitride semiconductor layer structure, as taught by Shur et al., in Shirai's device, in order to reduce the resistance and provide a higher output power and an excellent noise characteristic.

As for claim 2, the prior art combined device shows said semiconductor layer structure has an AlGaIn/GaN hetero structure (Shur: [0025], lines 6-8 and 15-17).

As for claim 3, the prior art combined device shows a thickness of said portion of said insulating film varies stepwise (Shirai: Fig. 1).

As for claim 6, the prior art combined device shows said insulating film is a SiO<sub>2</sub> film or a SiN film (Shur: [0029], lines 8-9).

As for claim 7, the prior art combined device shows said insulating film is a laminated layer of a SiO<sub>2</sub> film and a SiN film (Shur: [0029], lines 8-9).

As for claim 8, the prior art combined device shows a drain field plate electrode D2 connected to said drain electrode D is arranged on said insulating film 14 between said gate electrode G and said drain electrode D (Shirai: Fig. 1).

As for claim 9, Shirai and Shur et al. disclosed substantially the entire claimed invention, as applied to claims 1 and 4 above, except the size of said field plate portion does not exceed 70% of an interval between said gate electrode and said drain electrode.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include the size of said field plate portion does not exceed 70% of an interval between said gate electrode and said drain electrode, in order to optimize the performance of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Furthermore, it has been held in that the applicant must show that a particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Note that the law is replete with cases in which when the mere difference between the claimed invention and the prior art is some dimensional limitation or other variable within the claims, patentability cannot be found. The instant disclosure does not set forth evidence ascribing unexpected results due to the claimed dimensions. See *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338 (Fed. Cir. 1984), which held that the dimensional limitations failed to point out a feature which performed and operated any differently from the prior art.

As for claims 12 and 14, Shirai and Shur et al. disclosed substantially the entire claimed invention, as applied to claim 1 above, except the entire size of said field plate portion that extends to said drain electrode is 0.5  $\mu\text{m}$  or more and preferably 0.7  $\mu\text{m}$  or more.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include the entire size of said field plate portion that extends to said drain electrode is 0.5  $\mu\text{m}$  or more and preferably 0.7  $\mu\text{m}$  or more, in order to optimize the performance of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Furthermore, it has been held in that the applicant must show that a particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Note that the law is replete with cases in which when the mere difference between the claimed invention and the prior art is some dimensional limitation or other variable within the claims, patentability cannot be found. The instant disclosure does not set forth evidence ascribing unexpected results due to the claimed dimensions. See *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338 (Fed. Cir. 1984), which held that the dimensional limitations failed to point out a feature which performed and operated any differently from the prior art.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shirai (5,422,505) and Shur et al. (2005/0087752), as applied to claim 1 above, in view of Martinez et al. (2003/0235974).

Shirai and Shur et al. disclosed substantially the entire claimed invention, as applied to claim 1 above, except said insulating film is a SiON film.

Martinez et al. teach the insulating film 38 is a SiON film ([0017], line 1).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the SiON insulating layer, as taught by Martinez et al., in Shirai and Shur et al.'s device, in order in order to reduce parasitic capacitances and thus increase the device performance and reduce the power consumption of the device.

11. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shirai (5,422,505) and Shur et al. (2005/0087752), as applied to claim 1 above, in view of Riccobene (6,229,184).

Shirai and Shur et al. disclosed substantially the entire claimed invention, as applied to claim 1 above, except a thickness of said field plate portion gradually decreases from said gate electrode toward said drain electrode.

Riccobene teaches a thickness of said field plate portion gradually decreases from said gate electrode toward said drain electrode (Fig. 1).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include a thickness of said field plate portion gradually decreases from said gate electrode toward said drain electrode, as taught by Riccobene in Shirai and Shur et al.'s device, in order to reduce capacitance and increase circuit speed.

### ***Response to Arguments***

12. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **MEIYA LI** whose telephone number is (571)270-1572. The examiner can normally be reached on Monday-Friday 7:30AM-5:00PM Eastern Standard Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. L./  
Examiner, Art Unit 2811  
6/16/2008

/Ori Nadav/  
Primary Examiner, Art Unit 2811